UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,856	04/13/2004	James K. Jacobs	EV0302A	2661

7590 09/24/2007

David B. Woycechowsky
ELECTROVAYA, INC.
2645 Royal Windsor Drive
Mississauga, ON L5J 1K9
CANADA

EXAMINER	
RUTLAND WALLIS, MICHAEL	

ART UNIT	PAPER NUMBER
2836	

MAIL DATE	DELIVERY MODE
09/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,856	JACOBS ET AL.	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,7-40 and 55-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25,27-40,55-57 and 60-62* is/are rejected.

7)☒ Claim(s) *26,58 and 59* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicants addition of claims 55-62 filed with the submission on 08/24/2007 does not comply with the requirements of 37 CFR 1.121(c) (3) which states in relevant part:

(3) *When claim text in clean version is required.* The text of all pending claims not being currently amended shall be presented in the claim listing in clean version, *i.e.*, without any markings in the presentation of text. The presentation of a clean version of any claim having the status of "original," "withdrawn" or "previously presented" will constitute an assertion that it has not been changed relative to the immediate prior version, except to omit markings that may have been present in the immediate prior version of the claims of the status of "withdrawn" or "previously presented." **Any claim added by amendment must be indicated with the status of "new" and presented in clean version, *i.e.*, without any underlining.**

Applicant's submission neverthless has been entered, as it appeast Applicant has made a diligent effort to comply with 37 CFR 1.121(c).

In any further correspondence with the Office Applicant should review and comply with the requirements of 37 CFR 1.121(c) or the reply shall be held non-compliant.

Response to Arguments

Applicant's arguments with respect to the currently pending claims have been considered but are moot in view of the new grounds of rejection.

Claim Objections

Claim 60 recites, "A module comprising...", when Applicant refers to a module throughout the specification such as, in page 8 of the specification lines 15-20 recites when referring module shown in figure 2, as a highly integrated power management module. It therefore becomes unclear what difference if any there is between the highly integrated module as described in claim 60 and the single package housing recited in claims 61 and 62. It is suggest that Applicant amend the language "module" to "package".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7-22, 25 and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli (U.S. Pat. No. 6,975,098) in view of Shenai et al. (U.S. Pat. No. 5,959,439)

With respect to claims 1 and 55-57 Vinciarelli teaches a power supply system comprising; a first circuitry portion (for example 66A), the first circuitry portion

comprising at least one first power conversion switch (contained within the DC-DC converters items 48 and/or switching regulators 65 and/or other voltage transformation module seen detailed in Fig. 9) structured to perform power conversion switching to facilitate conversion of at least a first power input signal (Vf or Vin connected to the converter input) into a first power output signal (V1); a second circuitry portion (for example 66B), the second circuitry portion comprising at least one second power conversion switch (contained within the DC-DC converters items 48 and/or switching regulators 65) structured to perform power conversion switching to facilitate conversion of at least the first power input signal into a second power output signal (voltage input into the second power conversion module). Vinciarelli teaches a plurality of conversion circuits (see 42e) may be mounted on the package however is not directed toward specific output power conversion ratios (e.g. one third or one fourth power conversion) rather Vinciarelli simply notes the converter should convert the output voltage to that which required by the load citing several typical voltages in col. 2 such as: 2v, 5v and 12v. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to use the third, fourth and fifth modules to utilize a one third, one fourth and one fifth power conversion respectively in order to produce a plurality of voltages that may be used by different load found in a computer system. Vinciarelli further teaches the voltage transformation modules and conversions circuitry take up valuable space when placed onto isolated subassemblies (col. 11 line 1). Vinciarelli teaches voltage conversion circuitry for converting a voltage may be fit into a package or IC (col. 13 lines 29-30). Vinciarelli does not teach all the power conversion

switches for converting the input voltage are located within the package housing. Shenai teaches circuitry for voltage conversion may be monolithically fabricated as part of a multifunction chip (col. 2 lines 55-65). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to use a single package housing for first through fifth circuitry to convert the input voltage in order to minimize the required board and lead space taken by the circuitry and reduce construction and implementation costs

With respect to claims 7 and 8 Vinciarelli teaches the first power input signal is a dc signal (see voltage in); the first power output signal is a dc signal (DC to DC conversion output); and the second power output signal is a dc signal (DC to DC conversion output) or AC (see switching regulation circuitry).

With respect to claims 9 and 10 Vinciarelli teaches the at least one first and second power conversion switch is structured to perform efficient power conversion. Vinciarelli does not describe the conversion as ultra high efficiency. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify to Vinciarelli use more efficient switches if in fact the switches are not already considered ultra efficient in order to reduce excess heat.

With respect to claim 11 Vinciarelli teaches the at least one first power conversion switch is structured to perform at an efficient power conversion which one may construe a high or a low efficiency.

With respect to claim 12 Vinciarelli teaches the first module comprises at least two first power conversion switches (items 58 and 60 for example) structured to perform

power conversion switching to facilitate conversion of the first power input signal into the first power output signal; and the second module comprises at least two second power conversion switches structured to perform power conversion switching to facilitate conversion of the second power input signal into the second power output signal.

With respect to claims 13 and 14 Vinciarelli teaches the system is configured to provide power to diverse electrical components in an electronic system which one skilled in the art may construe a high or a low power.

With respect to claim 15 and 16 Vinciarelli teaches the first and second power conversion switches are operable so that the power output signal has an adjustable voltage output in the range of about +0.5 volts to +2.0 (col. 2 line 20-25) volts. Vinciarelli does not specifically citing the powering of the CPU with specifically 2 volts however it would have been obvious to one of ordinary skill in the art at the time of the invention to supply such a voltage to the core of the CPU in order for the CPU to receive the proper input voltage to perform properly.

With respect to claim 17-21 Vinciarelli teaches the output voltages are typical output voltages known to one skilled in the art citing several typical voltages in col. 2 such as: 2v, 5v and 12v. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to output any power conversion with a typical range of devices found in computing devices.

With respect to claim 22 Vinciarelli teaches the system comprises a bridge (i.e. is connected between the supply and load) between at least one power supply and a central processing unit (not shown).

With respect to claim 25 Vinciarelli teaches the conversion circuitry is contained within a package, further Shenai teaches the use of control circuitry used in voltage conversion is contained within a package. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to have control logic in the package as seen in Shenai in order to reduce the size and associated costs of a separately fabricated logic.

Claims 27-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli (U.S. Pat. No. 6,975,098) in view of Shenai et al. (U.S. Pat. No. 5,959,439) in further view of Wright (U.S. Pat. No. 6,541,879)

With respect to claims 27-28 and 29 Vinciarelli teaches does not detail the sub steps of sending and receiving power management signals through a USB. Wright teaches plural modules (110) mounted on a circuit connected to a USB management controller to send and receiving power management controls among other things. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to include the connection of such a control interface in order to supply multiple devices connected to a USB hub.

With respect to claim 31 Vinciarelli teaches does not detail the sub steps of sending and receiving power management signals through a embedded controller. Wright teaches plural modules (110) mounted on a circuit connected to an embedded management controller to send and receiving power management controls among other things. It would have been obvious to one of ordinary skill in the art at the time of the

invention to modify Vinciarelli to include the connection of such a control interface in order to supply multiple devices connected to a hub to increase power density.

With respect to claim 30 Vinciarelli teaches the use of a controller however does not teach the use of an I2C protocol. Wright teaches the power management commands are sent from the embedded controller to the control input/output port through serial bus. I2C is a well know protocol used to peripherals to a motherboard or the like and would have been obvious to one of ordinary skill in the art at the time of invention to utilize an I2C protocol in the command transmission in order to communicate with devices to reduce jitters in the connection.

With respect to claim 32 Vinciarelli teaches the use of a controller however does not teach the use of an I2C protocol. Wright teaches the power management commands are sent from the embedded controller to the control input/output port through serial bus. SMbus is a well know protocol used to peripherals to a motherboard or the like and would have been obvious to one of ordinary skill in the art at the time of invention to utilize an SMbus protocol in the command transmission in order to communicate with devices to reduce jitters in the connection.

With respect to claim 33 Vinciarelli teaches the system for a computing system and an on/off control block (130), located within the housing, the on/off control block being structured and located to initiate a power up process and supply power to the load. Vinciarelli does disclose the use of computer system. Wright teaches a control block and enable circuitry connected thereto. It would have been obvious to one of

ordinary skill in the art at the time of the invention to modify Vinciarelli to use such a control block to turn the power on and off when the power is not needed.

With respect to claim 34 Wright teaches the computer comprises an on/off switch; and the on/off control block comprises an on/off port for interfacing with the on/off switch.

With respect to claim 35 Wright teaches the on/off port is designed for ultra-low power consumption when the computer is in a power-off condition (no power is used).

With respect to claim 36 Vinciarelli teaches a controller may be embedded wherein Vinciarelli as modified by Wright teaches the on/off control block comprises power-up module structured and located to power up the controller.

Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli (U.S. Pat. No. 6,975,098) in view of Shenai et al. (U.S. Pat. No. 5,959,439) in further view of Klughart (U.S. Pat. No. 6,396,137)

With respect to claim 23 Vinciarelli as modified above teaches the system of claim 1 however does not teach the detailed manufacturing technique such a flip chip style die. Klughart teaches the use of a flip chip style die (Fig 26). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to use a flip chip style die in order to reduce manufacturing costs.

With respect to claim 24 Vinciarelli modified above teaches the mounting of the converters to subassemblies or ICs however does not illustrate the configuration at the die architecture level. Klughart teaches the semiconductor die level in Fig 26 for mounting a converter. It would have been obvious to one of ordinary skill in the art at

the time of the invention to modify Vinciarelli to use at least one semiconductor die in the first and second modules if in fact such is not already present in order to simply fabricate the converter.

Claims 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli (U.S. Pat. No. 6,975,098) in view of Kim et al. (U.S. Pat. No. 5,955,797)

With respect to claim 37 Vinciarelli teaches the system on claim 1 however does not teach the further inclusion of a battery and detailed charging outputs. Kim teaches a first battery (battery within battery pack item 20); a first battery-charging output (item 100), the first battery charging output having an adjustable voltage and current suitable for charging the first battery; a first battery current path structured and located to electrically connect the first battery and the first battery-charging output so that the first battery can be charged by electrical power from the first battery-charging output. It would have been obvious to one of ordinary skill in the art at the time of the invention to battery pack and charging output located on the package of the Vinciarelli in order to provide regulated power to charge the batteries of a laptop computer.

With respect to claim 38 Kim teaches the use of a communication and control channel to charging circuit see output of item 120 connected to the charging circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to include use a serial communication interface to control the charging current to the battery.

With respect to claim 39 Kim teaches a battery pack known to contain plural batteries however depicts only one output to the charge the battery. It would have been

obvious to one of ordinary skill in the art at the time of the invention to modify Kim to duplicate the battery and charger to include a second battery and battery charging unit in order to have a redundant battery system and charging line.

With respect to claim 40 Vinciarelli teaches the use of voltage transformers and output lines associated with the transformers, however is silent on the particular loads connected thereto. Kim teaches the use of an inverter to transformer the output power to power a backlight for a display. It would have been obvious to one of ordinary skill in the art at the time of the invention to include such an AC output line a on the package of the Vinciarelli in order to provide regulated power to provide a regulated voltage to a display of a computing system.

Claim 60 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli (U.S. Pat. No. 6,975,098) in view of Barnes et al. (U.S. Pat. No. 7,119,458) in view of Christensen (U.S. Pat. No. 6,703,722)

With respect to claim 60 Vinciarelli teaches a module comprising the following: a first circuitry portion (for example 66A), the first circuitry portion comprising at least one first power conversion switch (contained within the DC-DC converters items 48 and/or switching regulators 65 and/or other voltage transformation module seen detailed in Fig. 9) structured to perform power conversion switching to facilitate conversion of at least a first power input signal (Vf or Vin connected to the converter input) into a first power output signal (V1); a second circuitry portion (for example 66B), the second circuitry portion comprising at least one second power conversion switch (contained within the DC-DC converters items 48 and/or switching regulators 65) structured to perform power

conversion switching to facilitate conversion of at least the first power input signal into a second power output signal (voltage input into the second power conversion module), a power converter switch controller (see Fig. 9) structured, electrically connected and to control the power conversion related switching of the first switching power converter, the second switching power converter and the third switching power converter. Vinciarelli does not teach the use of detail the use of input circuitry to couple to first and second batteries. Barnes teaches the use of adapters and circuitry to couple to an AC input, a first battery, a second battery. Barnes further teaches the use of an input power controller structured which may be select among a plurality of input signals and output a conditioned voltage signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to include input circuitry to connect to first and second batteries in order to supply backup power when the AC is absent. Neither Vinciarelli nor Barnes teaches the use of a distribution controller. Christensen teaches the use if output switching circuitry control distribution of at least the first power output signal, the second power output signal and the third power output signal to external loads. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli and Barnes to include power distribution circuitry in order to determine the load from which the supply is powered.

Claims 61-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vinciarelli (U.S. Pat. No. 6,975,098) in view of Barnes et al. (U.S. Pat. No. 7,119,458) in view of Christensen (U.S. Pat. No. 6,703,722) in further view of Shenai et al. (U.S. Pat. No. 5,959,439) Vinciarelli further teaches the voltage transformation modules and

conversions circuitry take up valuable space when placed onto isolated subassemblies (col. 11 line 1). Vinciarelli teaches voltage conversion circuitry for converting a voltage may be fit into a package or IC (col. 13 lines 29-30). Vinciarelli does not teach all the power conversion switches for converting the input voltage are located within the package housing. Shenai teaches circuitry for voltage conversion may be monolithically fabricated as part of a multifunction chip (col. 2 lines 55-65). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Vinciarelli to use a single package housing for first through fifth circuitry to convert the input voltage in order to minimize the required board and lead space taken by the circuitry and reduce construction and implementation costs

Allowable Subject Matter

Claim 26, 58-59 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 26 Vinciarelli as modified in claim 25 teaches the voltage conversion circuitry however does not further teach the control port to receive communication signal from outside of the package housing, wherein: a mode of the first, second, third, fourth and fifth power conversion switches is determined by the communication signal; and the operation of the first, and second, third, fourth and filth

switch drivers is controlled by the control logic block based at least in part by the mode. At least this further limitation is not taught or rendered obvious by the prior art of record.

With respect to claim s 58 and 59 Vinciarelli as modified in claim 55 teaches the system however does not teach the structuring to perform power conversion switching to selectively convert a third power input signal into the first power output signal; and to perform power conversion switching to selectively convert the third power input signal into the second power output signal. At least this further limitation is not taught or rendered obvious by the prior art of record.

Conclusion

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MRW

9/15/07

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER